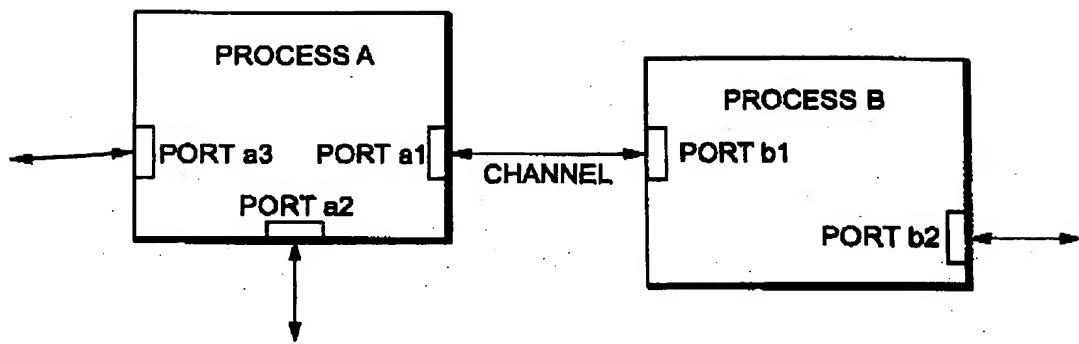
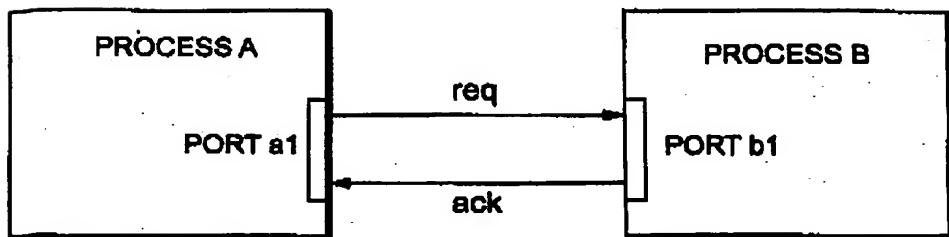


Fig.1



INTERPROCESS COMMUNICATION

Fig.2



INTERPORT COMMUNICATION

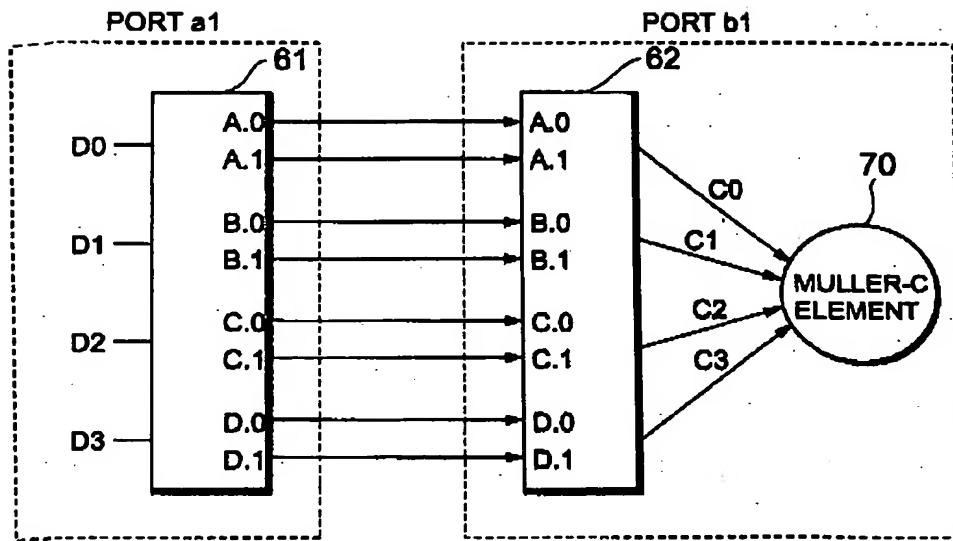
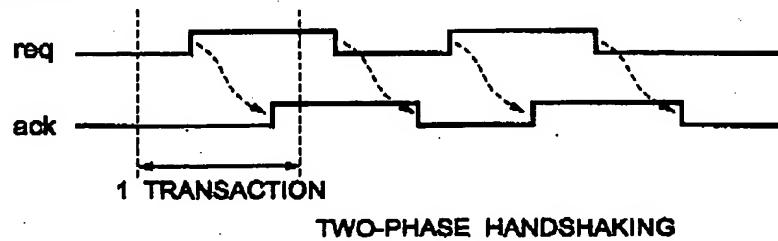
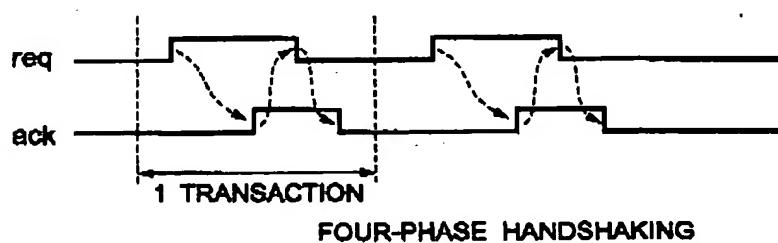
Fig. 3CONSTITUTIONAL VIEW OF CIRCUIT FOR REMOVING
PASSIVE CLOCKING**Fig. 4A****Fig. 4B**

Fig. 5

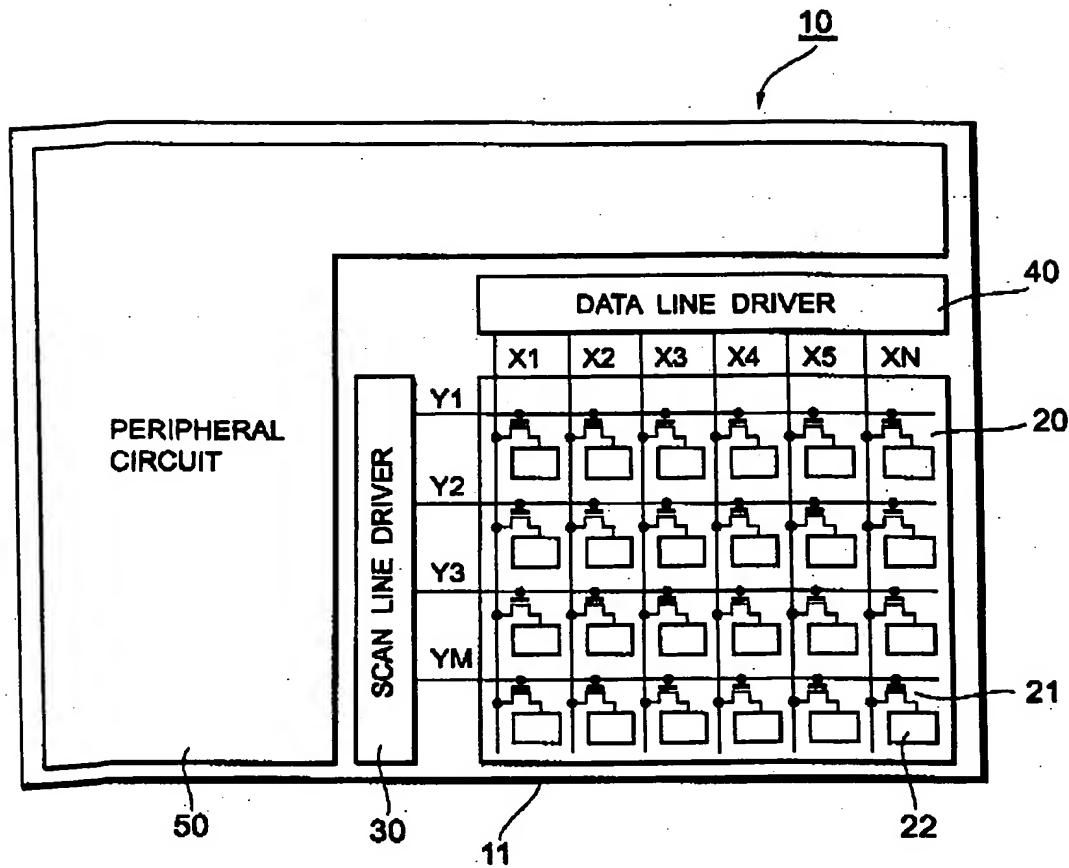


Fig. 6

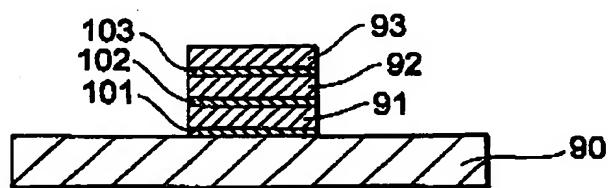


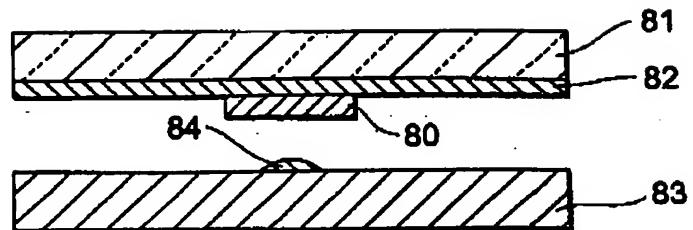
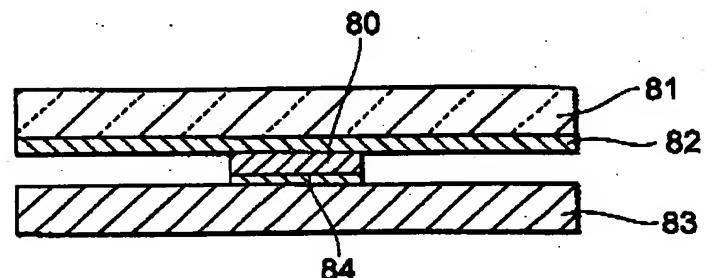
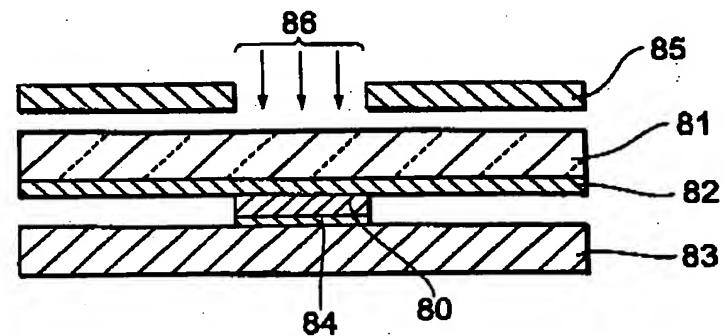
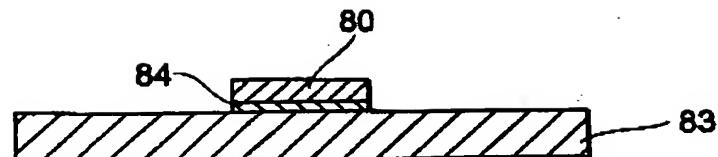
Fig.7A**Fig. 7B****Fig. 7C****Fig. 7D**

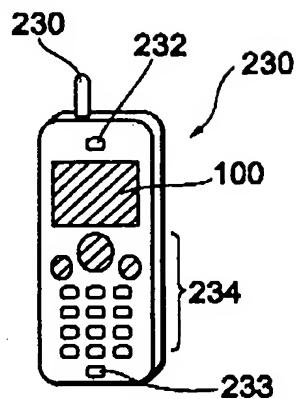
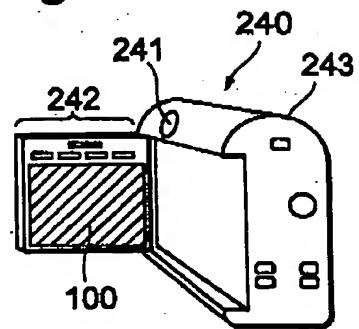
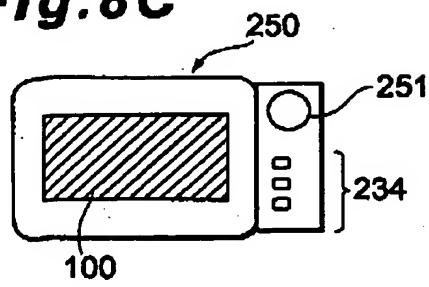
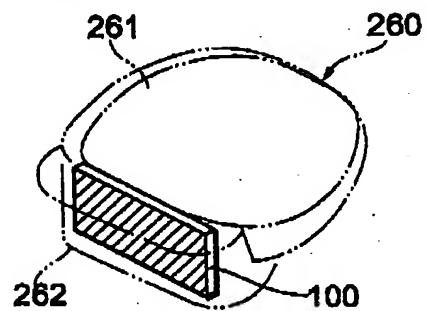
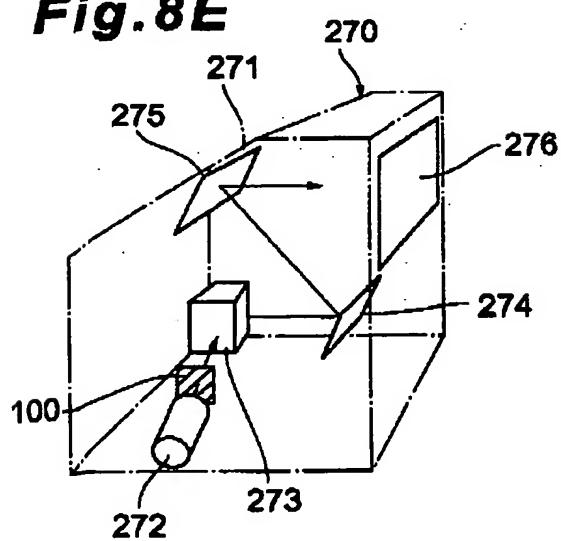
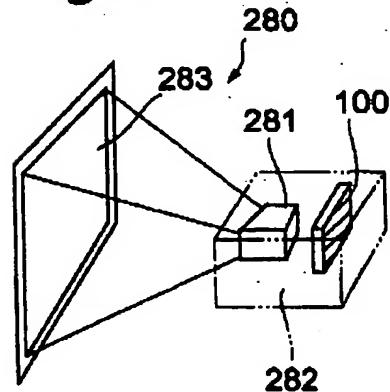
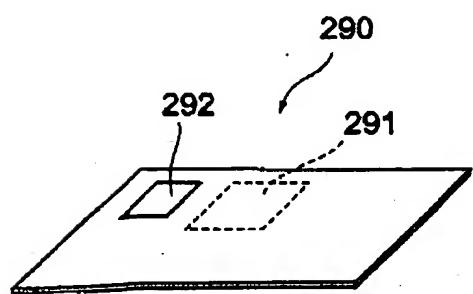
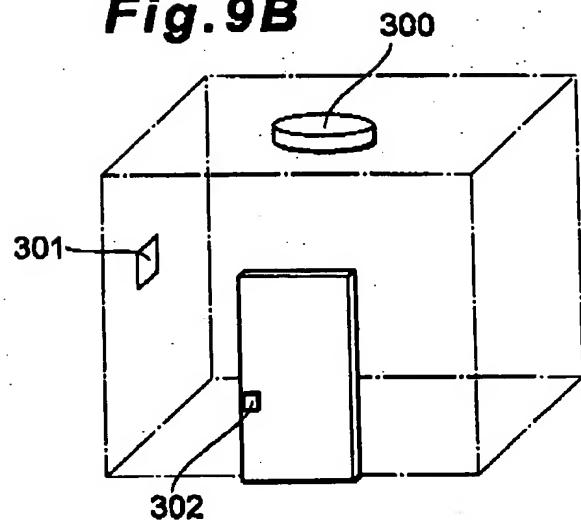
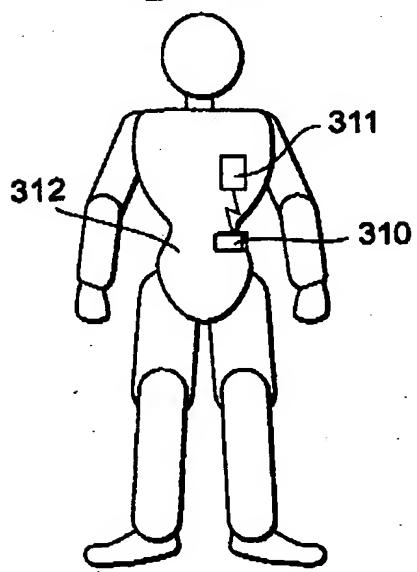
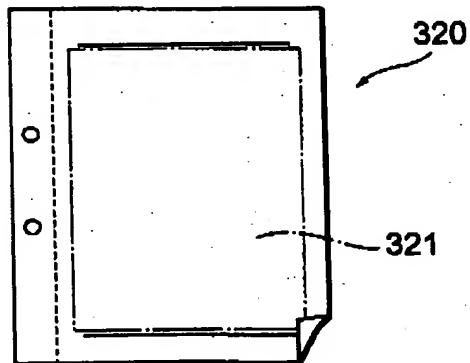
Fig. 8A**Fig. 8B****Fig. 8C****Fig. 8D****Fig. 8E****Fig. 8F**

Fig.9A**Fig.9B****Fig.9C****Fig.9D**

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Fig.9E